REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-31 remain pending in the application. By this Amendment, the specification is amended to identify the co-pending patent application number; and claims 1 and 17 are amended. No new matter is added.

In numbered paragraph 3 of the Office Action, independent claims 1 and 17, along with various dependent claims, are rejected under 35 U.S.C. §103 as being unpatentable over JP 409022380 A (Kimura) in view of JP 408272756 A (Yamagami et al.) and U.S. Patent 5,502,718 (Lane et al.). In numbered paragraph 4 of the Office Action, dependent claims 19-26 and 28-31 are rejected under 35 U.S.C. §103 as being unpatentable over the Kimura publication in view of the Yamagami et al. publication and the Lane et al. patent, and further in view of Shanley et al., PCI System Architecture, Third Edition, Mind Share, Inc., 1995, pp. 39-45 and 76-89. In numbered paragraph 5 of the Office Action, dependent claims 8-13 are rejected under 35 U.S.C. §103 as being unpatentable over the Kimura publication in view of the Yamagami et al. publication and the Lane et al. patent, and further in view of U.S. Patent 5,990,939 (Sand et al.). In numbered paragraph 6 of the Office Action, dependent claim 27 is rejected under 35 U.S.C. §103 as being unpatentable over the Kimura publication in view of the Yamagami et al. publication, the Lane et al. patent and the Shanley et al. article, and further in view of U.S. Patent 6,138,176 (McDonald et al.). These rejections are respectfully traversed.

Applicant has disclosed a method and apparatus for managing flow of information among plural processors of a processing array. The flow of data and control packet information is managed among plural processors by connecting

processors within modules on a local bus, which is then connected to the system bus by way of a gateway (e.g., paragraphs [0027] and [0028]). The system bus 102 is the primary control and data path of the processor subsystem (e.g., paragraph [0027]). A system bus arbitration unit 112 of the system controller is provided for arbitrating access to the system bus by the various modules (e.g., paragraph [0026]). The system controller initiates and performs control actions. A clear path is established between various modules or devices contained on the system bus, and processors contained within modules located on local buses (e.g., paragraph [0007]).

The foregoing features are broadly encompassed by claim 1, which recites, among other features, an apparatus for managing flow of information among plural processors of a processing array, including a system bus for interconnecting at least two processors and providing a path for packets of data and control information; and means for arbitrating access to at least a first portion of the system bus among said at least two processors to transfer said packets of data and control information over said first portion, said means for arbitrating establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy, and said packets being transferred using a protocol by which the system bus performs control actions for system bus access independently of said at least two processors.

On page 2 of the Office Action, the Examiner admits that the Kimura publication does not teach means for arbitrating access to at least a first portion of a system bus. On page 3 of the Office Action, the Examiner admits that "Kimura, as modified by Yamagami, does not teach said means for arbitrating establishing a

clear path to a destination device by checking device busy signals to ensure that said destination device is not busy."

The Lane et al. patent, considered individually or in combination with the Kimura and Yamagami et al. publications, does not teach or suggest means for arbitrating access to at least a first portion of a system bus among at least two processors to transfer packets of data and control information over the first portion, the means for arbitrating establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy. The Lane et al. patent discloses data packets exchanged through paths 26, 27 and buffers 28, 29 (col. 6, lines 47-60) that are separate and distinct from the command information paths 211, 214, 215 and their command modules 23, 210 (e.g., col. 7, lines 23-46; Fig. 2). Further, the Lane et al. disclosure does not teach or suggest that these command buffers 211, 214, 215 transfer packets. At least for the foregoing reasons, the Lane et al. patent does not cure the deficiencies of the Kimura and Yamagami et al. publications.

The Sand et al. patent, the Shanley et al. article, and the McDonald et al. patent, considered individually or in combination with the Kimura and Yamagami et al. publications and the Lane et al. patent, do not cure the deficiencies of the Kimura and Yamagami et al. publications and the Lane et al. patent. The Sand et al. patent was cited for its disclosure of a video thermal tracker interface 70 shown in Fig. 2, the Shanley et al. article was cited for its disclosure of a PCI bus operation and arbitration, and the McDonald et al. patent was cited for its disclosure of a round robin arbitration protocol (abstract; see, also, separate switched 90 and control 86 buses in Fig. 2). However, the Sand et al. patent, the Shanley et al. article, and the

McDonald et al. patent, considered individually or in combination with the Kimura and Yamagami et al. publications and the Lane et al. patent, do not teach or suggest means for arbitrating access to at least a first portion of a system bus among at least two processors to transfer packets of data and control information over the first portion, the means for arbitrating establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy.

For the foregoing reasons, Applicant's claims 1 and 17 are allowable. The remaining claims depend from independent claims 1 and 17, and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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